

Voltage Balancing Technique Using Z-S Voltage and N-S current for Cascaded H-bridge STATCOM

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ABSTRACT:

This paper presents a control scheme of cascaded H-bridge STATCOM in three-phase powersystems. The phase cluster of STATCOM consists of there H-bridge cells connected in series. The feature is that each H-bridge cell generates a different output voltage $v_c, 2v_c, 4v_c$. By this each phase cluster can generate 15-level output voltage. According to this configuration every H-bridge cell has isolated dc capacitors. So the balancing problem of capacitor voltages exists. Since STATCOM is often requested to operate under asymmetrical condition by power system faults such as one line grounding or two-line short circuit.

Recently, several methods of voltage balancing between phase clusters are proposed. One method is based on zero-sequence voltage injection. However it needs wide margin of dc capacitor voltage compared with rated power system voltage when the unbalance of power system voltage is large. We also had proposed a capacitor voltage balancing method using negative-sequence current. However the output current of the STATCOM using the method is uniquely determined by the unbalance of power system voltage and function of the STATCOM is limited. To solve this problem, a technique using zero sequence voltage and negative-sequence current is proposed. By this scheme, the STATCOM is allowed to operate under asymmetrical conditions by power system faults. The validity is examined by digital simulation.

Key Words: Capacitor voltage balancing, Cascaded H-bridge, multilevel converter, STATCOM, Zero-sequence voltage.

1. INTRODUCTION

CASCADED H-bridge multilevel converter consists of series connected H-bridge cells. It has merits of switching losses of semiconductor device and harmonics in output voltage. And it is considered to be suitable for STATCOM in power system application, because it requires less number of circuit components compared with diode-clamped multilevel converter or flying capacitor multilevel converter and STATCOM does not have to handle real power.

But every H-bridge cell has isolated dc capacitor and balancing problem of capacitor voltages exists in this configuration. STATCOM is often requested to operate under asymmetrical condition by power system faults, such as one line grounding or two-line short circuit. These kinds of faults cause unbalance of power system voltage and unbalance current flows into each phase cluster. So capacitor voltage balancing between phase clusters is particularly important.

Recently, several methods of voltage balancing between phase clusters are proposed. One method is based on zero-sequence voltage injection. However it needs wide margin of dc capacitor voltage compared with rated power system voltage when the unbalance of power system voltage is large. The other method handles the capacitor voltage unbalance by independently controlling active power of individual phase cluster, but unbalance of power system voltage is not considered. By these reasons, the circuit condition in which these methods are effective is considered to be limited in practical use

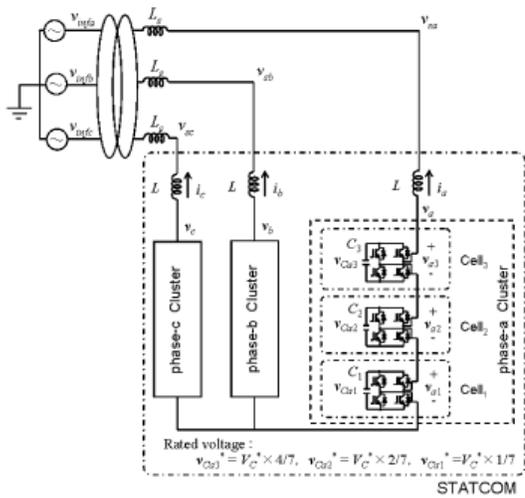
We also had proposed a capacitor voltage balancing method using negative-sequence current. It does not need wide margin of dc capacitor voltage and can handle large unbalance of power system voltage. However the output current of the STATCOM using the method is uniquely determined by the unbalance of power system voltage and function of the STATCOM is limited

So we introduce a different control method using zero-sequence voltage in this paper. By this method, the STATCOM can control output current almost freely. But it needs wide margin of dc voltage under large power system voltage unbalance. To avoid this, we exclusively use the two methods depending on the extent of voltage unbalance. The validity is examined by digital simulation under one-line and two-lines fault circuit condition.

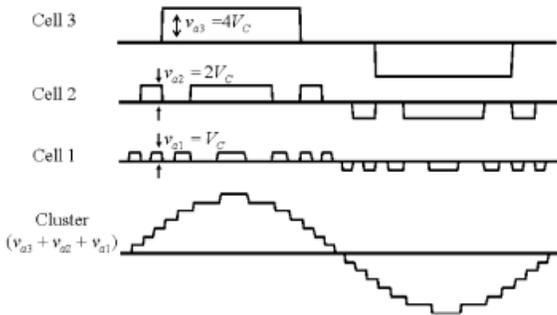
2. MAIN CIRCUIT AND CONTROL SCHEME

2.1. MAIN CIRCUIT AND BASIC OPERATION

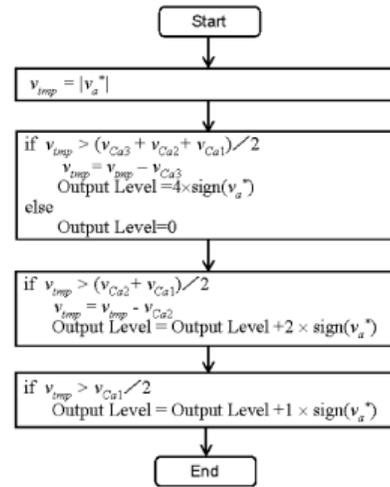
Fig. 1(a) shows the main circuit of cascaded H-bridge STATCOM in this paper. It is composed of three-phase clusters. Each phase cluster consists of three H-bridge cells. The dc capacitor voltages are set to V_C , $2V_C$, $4V_C$ in a phase cluster. Fig. 1(b) shows an example of output waveform. Voltage level from -7 to +7 can be generated by combining the capacitor voltages. The level is decided according to the calculation flow shown in Fig. 1(c). Then the cluster outputs the nearest voltage level to reference V_a^* .



(a)



(b)



(c)

Fig.1.circuit configuration and operation (a) Main circuit.(b) Example of output waveform. (c) Decision method of output level.

Conventional cascaded H-bridge multilevel converter may require high number of H-bridge cells for low current distortion. But the proposed circuit configuration can output 15-level voltage in spite of only three cells. So, lower conduction losses of semiconductor devices are expected.

For dc voltage balancing in each phase cluster, the control method proposed here uses the fact that several switching patterns are available when a phase cluster outputs particular voltage levels. An example is shown in Fig. 2. When a phase cluster outputs voltage V_C , there exists three operational pattern “ V_C ”, “ $2V_C - V_C$ ”, and “ $4V_C - 2V_C - V_C$ ” and charged or discharged capacitors are different. These patterns are selected According to the relation between V_{C1} , V_{C2} and V_{C3} . When $4V_{C1} \geq 2V_{C2}$, and V_{C3} , output pattern “ V_C ” is selected. When $2V_{C2} > 4V_{C1}$ and V_{C3} , output pattern “ $2V_C - V_C$ ” is selected. When $V_{C3} > 2V_{C2}$ and $4V_{C1}$, output pattern “ $4V_C - 2V_C - V_C$ ” is selected. To use same switching pattern in $1/4$ cycle, the capacitor voltages are measured at $0.\pi/2$, $3\pi/2$ [rad] of ac side phase angle.

Table I Decision Table of Operation Pattern for Voltage Balancing

Output Level	Cell ₃	Cell ₂	Cell ₁	Condition
1			1	$4v_{C1} \geq 2v_{C2}$ and $4v_{C1} \geq v_{C3}$
	1	1	-1	$2v_{C2} \geq v_{C3}$ and $2v_{C2} > 4v_{C1}$
	1	-1	-1	$v_{C3} > 4v_{C1}$ and $v_{C3} > 2v_{C2}$
2		1		$2v_{C2} \geq v_{C3}$
	1	-1		$2v_{C2} < v_{C3}$
3		1	1	$2v_{C2} \geq v_{C3}$ and $4v_{C1} \geq v_{C3}$
	1		-1	$v_{C3} > 4v_{C1}$ and $2v_{C2} > 4v_{C1}$
	1	-1	1	$v_{C3} > 2v_{C2}$ and $4v_{C1} \geq 2v_{C2}$
4	1			
5	1		1	$4v_{C1} \geq 2v_{C2}$
	1	1	-1	$4v_{C1} < 2v_{C2}$
6	1	1		
7	1	1	1	

Table I shows the all operational patterns and decision method. It is used when the polarities of STATCOM output voltage and current are same. "1" indicates that the cell outputs voltage to positive direction and its capacitor is discharged.

"-1" indicates that the cell output voltage to negative direction and its capacitor is charged. It is similar when the polarity of the output current is opposite. By this method, capacitor voltage ratio between H-bridge cells in a phase cluster is controlled.

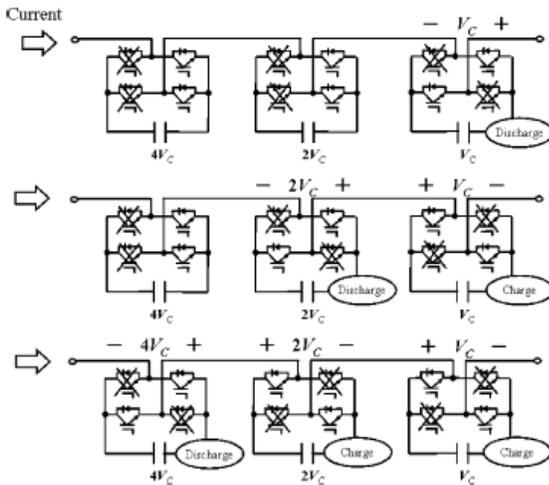


Fig. 2. An example of capacitor voltage balancing between H-bridge cells.

2.2. CAPACITOR VOLTAGE BALANCING BETWEEN PHASE CLUSTERS

STATCOM is often requested to operate under asymmetrical condition by power system faults, such as one line grounding or two-line short circuit. These kinds of faults cause unbalance of power system voltage and unbalance current flows into each phase cluster. Then capacitor voltage unbalance between phase clusters occurs.

So we had proposed a capacitor voltage balancing method using negative-sequence current. The negative-sequence current. The negative -sequence current i_{na} , i_{nb} , i_{nc} for capacitive voltage balancing is expressed as

$$\begin{pmatrix} i_{na} \\ i_{nb} \\ i_{nc} \end{pmatrix} = \sqrt{\frac{2}{3}} k_n v_{ca} \begin{pmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \end{pmatrix} + \sqrt{\frac{2}{3}} k_n v_{cb} \begin{pmatrix} \cos(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t) \end{pmatrix} + \sqrt{\frac{2}{3}} k_n v_{cc} \begin{pmatrix} \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \end{pmatrix} \quad (1)$$

Where K_n is a gain, and V_{ca}, V_{cb}, V_{cc} , are the sum of capacitor voltages in a phase cluster, as shown

$$\begin{aligned} v_{ca} &= \sum_{k=1,2,3} v_{cak} \\ v_{cb} &= \sum_{k=1,2,3} v_{cbk} \\ v_{cc} &= \sum_{k=1,2,3} v_{cck} \end{aligned} \quad (2)$$

Here, it is assumed that the STATCOM shown in Fig. 1 operates under the asymmetrical circuit condition, as shown

$$\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} = \sqrt{\frac{2}{3}} v_p \begin{pmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \end{pmatrix} + \sqrt{\frac{2}{3}} v_n \begin{pmatrix} \cos(\omega t + \theta) \\ \cos(\omega t + \frac{2\pi}{3} + \theta) \\ \cos(\omega t - \frac{2\pi}{3} + \theta) \end{pmatrix} \quad (3)$$

And its output current is controlled as shown in (4). Where, the first term is the active current to compensate converter losses. The second term is the reactive current output to power system. The third term is the negative-sequence current for

voltage balancing, as shown in (1)

$$\begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} = \sqrt{\frac{2}{3}} i_{pd}^* \begin{pmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \end{pmatrix} + \sqrt{\frac{2}{3}} i_{pq}^* \begin{pmatrix} -\sin(\omega t) \\ -\sin(\omega t - \frac{2\pi}{3}) \\ -\sin(\omega t + \frac{2\pi}{3}) \end{pmatrix} + \begin{pmatrix} i_{na} \\ i_{nb} \\ i_{nc} \end{pmatrix} \quad (4)$$

Then, the average real powers of each phase clusters are calculated as

$$\begin{pmatrix} P_a \\ P_b \\ P_c \end{pmatrix} = \begin{pmatrix} \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{3}} v_a \cdot i_a dt \\ \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{3}} v_b \cdot i_b dt \\ \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{3}} v_c \cdot i_c dt \end{pmatrix} = \frac{v_p k_n}{2} \begin{pmatrix} v_{ca} - v_c \\ v_{cb} - v_c \\ v_{cc} - v_c \end{pmatrix} + \begin{pmatrix} p \\ p \\ p \end{pmatrix} + \begin{pmatrix} P_{na} \\ P_{nb} \\ P_{nc} \end{pmatrix} \quad (5)$$

Where

$$v_c = \frac{v_{ca} + v_{cb} + v_{cc}}{3} \quad (6)$$

$$p = \frac{v_p i_{pd}^*}{3} + \frac{v_n k_n}{3} \begin{bmatrix} v_{ca} \cos \vartheta + v_{cb} \cos(\vartheta - \frac{2\pi}{3}) \\ + v_{cc} \cos(\vartheta + \frac{2\pi}{3}) \end{bmatrix} \quad (7)$$

$$\begin{aligned} P_{na} &= \frac{v_n i_{pd}^*}{3} \cos(\vartheta) + \frac{v_n i_{pq}^*}{3} \sin(\vartheta) \\ P_{nb} &= \frac{v_n i_{pd}^*}{3} \cos(\vartheta - \frac{2\pi}{3}) + \frac{v_n i_{pq}^*}{3} \sin(\vartheta - \frac{2\pi}{3}) \\ P_{nc} &= \frac{v_n i_{pd}^*}{3} \cos(\vartheta + \frac{2\pi}{3}) + \frac{v_n i_{pq}^*}{3} \sin(\vartheta + \frac{2\pi}{3}) \end{aligned} \quad (8)$$

In (5), the first term is proportional to the error between the individual capacitor voltage V_{Ca}, V_{Cb}, V_{Cc} and the average capacitor voltage V_c expressed as (6) and (2). The second term is the same for each phase cluster. The third term is almost independent of V_{Ca}, V_{Cb}, V_{Cc} as expressed in (8). So the error of the individual capacitor voltage is decreased by use of the negative-sequence current, i_{na}, i_{nb}, i_{nc} shown in (1).

Besides i_{na}, i_{nb}, i_{nc} can be expressed on dq-axes, as shown

$$\begin{pmatrix} i_{nd}^* \\ i_{nq}^* \end{pmatrix} = \begin{pmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{pmatrix} K_n \begin{pmatrix} v_{ca} - \frac{v_{cb} + v_{cc}}{2} \\ \frac{\sqrt{3}}{2}(v_{cc} - v_{cb}) \end{pmatrix} \quad (9)$$

So PI controller is actually used to calculate i_{nd}^*, i_{nq}^* in the control block of proposed STATCOM, instead of gain K_n , to make the error between the individual capacitor voltage and the average capacitor voltage zero, as shown in Fig. 3.

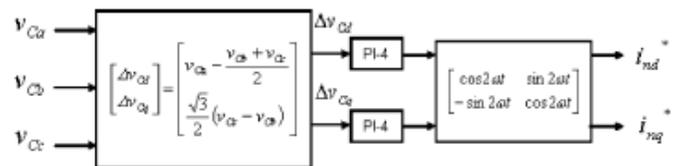


Fig.3. Calculation method of negative-sequence current for voltage balancing between phase clusters.

However the output current of the STATCOM using the negative- sequence current method is uniquely determined by unbalance of power system voltage and function of the STATCOM is limited. For example, the STATCOM becomes impossible to compensate negative-sequence current by unbalanced loads. So we introduce a different control method using zero-sequence voltage in this paper.

The zero-sequence voltage for capacitor voltage V_o balancing is expressed

$$v_o = \frac{\Delta P_a (i_a \cdot i_b) i_c + \Delta P_a (i_c \cdot i_a) i_b + \Delta P_a (i_a \cdot i_b) i_c}{|i_a|^2 |i_b|^2 - (i_a \cdot i_b)^2}$$

$$\Delta P_a = v_a' \cdot i_a - \frac{1}{3} \sum_{k=a,b,c} v_k' \cdot i_k$$

$$+ K_{op} \left(\frac{1}{3} \sum_{k=a,b,c} \sum_{j=1,2,3} \frac{1}{2} C_j v_{ckj}^2 - \sum_{j=1,2,3} \frac{1}{2} C_j v_{caj}^2 \right)$$

$$\Delta P_b = v_b' \cdot i_b - \frac{1}{3} \sum_{k=a,b,c} v_k' \cdot i_k$$

$$+ K_{op} \left(\frac{1}{3} \sum_{k=a,b,c} \sum_{j=1,2,3} \frac{1}{2} C_j v_{ckj}^2 - \sum_{j=1,2,3} \frac{1}{2} C_j v_{cbj}^2 \right)$$

$$\Delta P_c = v_c' \cdot i_c - \frac{1}{3} \sum_{k=a,b,c} v_k' \cdot i_k$$

$$+ K_{op} \left(\frac{1}{3} \sum_{k=a,b,c} \sum_{j=1,2,3} \frac{1}{2} C_j v_{ckj}^2 - \sum_{j=1,2,3} \frac{1}{2} C_j v_{ccj}^2 \right)$$

(10)

Where V_a', V_b', V_c' are positive and negative- sequence components of STATCOM output voltage i_a, i_b, i_c are STATCOM output current, K_{op} is a gain, operator “.” means scalar product of complex vector. To handle instantaneous value at time, it is substituted by the calculation as follows:

$$X.Y = \frac{\omega}{2\pi} \int_{t - \frac{2\pi}{\omega}}^t x(T) \times y(T) dT.$$

(11)

Where x and y are arbitrary phasor in (10) and x(t) and y(t) are their instantaneous value. ω is angular frequency of power system.

By using V_o shown in (10), STATCOM output power from each phase is calculated as follows. From (12), it is understood that the STATCOM outputs same power from each phase when the capacitor voltage of each phase is balanced. Even if capacitor voltage unbalance occurs, it is corrected by the second term of (12). It can be easily confirmed that the time constant to correct the capacitor voltage unbalance is $1/K_{op}$.

$$P_a = (v_a' + v_o) \cdot i_a = v_a' \cdot i_a - \Delta P_a$$

$$= \frac{1}{3} \sum_{k=a,b,c} v_k' \cdot i_k + k_{op} \left[\sum_{j=1}^3 \frac{1}{2} C_j v_{caj}^2 - \frac{1}{3} \sum_{k=a,b,c} \sum_{j=1}^3 \frac{1}{2} C_j v_{ckj}^2 \right]$$

$$P_b = (v_b' + v_o) \cdot i_b = v_b' \cdot i_b - \Delta P_b$$

$$= \frac{1}{3} \sum_{k=a,b,c} v_k' \cdot i_k + k_{op} \left[\sum_{j=1}^3 \frac{1}{2} C_j v_{cbj}^2 - \frac{1}{3} \sum_{k=a,b,c} \sum_{j=1}^3 \frac{1}{2} C_j v_{ckj}^2 \right]$$

$$P_c = (v_c' + v_o) \cdot i_c = v_c' \cdot i_c - \Delta P_c$$

$$= \frac{1}{3} \sum_{k=a,b,c} v_k' \cdot i_k + k_{op} \left[\sum_{j=1}^3 \frac{1}{2} C_j v_{ccj}^2 - \frac{1}{3} \sum_{k=a,b,c} \sum_{j=1}^3 \frac{1}{2} C_j v_{ckj}^2 \right]$$

(12)

However, this method requires a wide dc voltage margin. For example, it is assumed that two-line short circuit occurs in power system and positive and negative sequence of STATCOM output voltage becomes

$$v_a' = 1 + j0$$

$$v_b' = -0.5 + j0$$

$$v_c' = -0.5 + j0$$

(13)

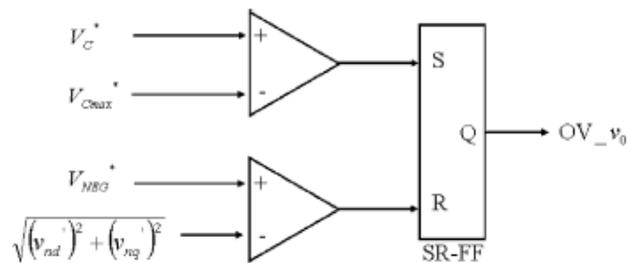


Fig. 4. Decision method of voltage balancing between phase clusters.

At this time, V_o shown in (10) is calculated as follows

$$V_o = 0.5 + j0$$

(14)

Then, the STATCOM output voltage becomes as follows:

$$\begin{pmatrix} V_{p\alpha} \\ V_{p\beta} \end{pmatrix} = \frac{1}{2} \begin{pmatrix} V_{\alpha} - V'_{\beta} \\ V_{\beta} + V'_{\alpha} \end{pmatrix} = V_P \begin{pmatrix} \cos \omega t \\ \sin \omega t \end{pmatrix}$$

$$\begin{pmatrix} V_{n\alpha} \\ V_{n\beta} \end{pmatrix} = \frac{1}{2} \begin{pmatrix} V_{\alpha} + V'_{\beta} \\ V_{\beta} - V'_{\alpha} \end{pmatrix}$$

$$= V_P \begin{pmatrix} \cos(\omega t + \mathcal{G}_n) \\ -\sin(\omega t + \mathcal{G}_n) \end{pmatrix} \quad (18)$$

$$\max_{k=a,b,c} \left(\sqrt{2} \times \sqrt{\frac{1}{T} \int_{t-T}^t v_k^*(\tau)^2 d\tau} \right) \xrightarrow{\text{LPF.2}} \times \frac{7}{6.5} \rightarrow V_C^*$$

Fig.6. Calculation method of capacitor voltage reference

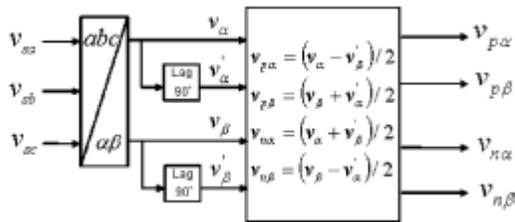


Fig.7. Decomposition from grid voltage to positive and negative sequence.

The feature of this method is that the appropriate values of $V_{p\alpha}$, $V_{p\beta}$, $V_{n\alpha}$, $V_{n\beta}$ are obtained in about 1/4 cycle even if sudden change of V_{α} , V_{β} occurs by power system faults. After dq-transformation of $V_{p\alpha}$, $V_{p\beta}$ and low pass filtering, the positive sequence voltage V_{pd} , V_{pq} are obtained as dc components. On the other hand, $V_{n\alpha}$, $V_{n\beta}$ are once rotated to reverse direction of transformation. Here, the negative-sequence voltage is also obtained as dc components. After low pass filtering, the output values are rotated two times to forward direction of transformation and the negative-sequence voltage V_{nd} , V_{nq} are obtained accurately

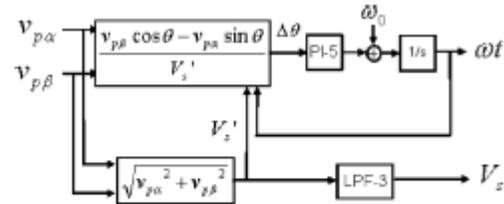


Fig.8. phase angle and voltage detection method.

The time constant of low pass filter does not have to be long, i.e. the delay time of low pass filter is not long, because the filter is requested to eliminate only harmonic component of ac side voltage. As a result, the STATCOM can respond to power system faults quickly, and the error of capacitor voltage between phase clusters is expected to be small even in the transient state by the faults. In addition $V_{p\alpha}$, $V_{p\beta}$ are used for PLL, shown in Fig. 8, to synchronize the phase angle ωt to positive sequence of the grid voltage. And the positive sequence voltage V_S at grid point is also obtained by this control block diagram.

Table II Circuit Parameters

Rated AC Voltage	V_C^*	3 ϕ AC 6600V
Rated Reactive Power	Q	1MVA
Line angular frequency	ω_0	$2\pi \times 60$ rad/s
Line Inductance	L_s	4.64mH (4%)
AC link Inductance	L	11.6mH (10%)
DC Capacitance	C_3	1mF
	C_2	2mF
	C_1	4mF
Rated Capacitor Voltage	v_{C3}^*	3900V
	v_{C2}^*	1950V
	v_{C1}^*	975V

3. SIMULATION RESULT

Digital simulation using EMTP(Electro Magnetic Transient Analysis Program) has been carried out to verify the effectiveness of the proposed scheme for the circuit shown in Fig. 1. The circuit parameters are given in Table II. Rated reactive power is 1 MVA. The sum of rated capacitor voltage $825V+1650V+3300V=5775$ is slightly higher than the

peak voltage of ac system, which is $\sqrt{\frac{2}{3}} \times 6000 \approx 5389V$. The

capacitance 1 mF, 2 mF, 4 mF are chosen so that the capacitor voltage ripple are less than about 5% of their rated voltage at outputting rated reactive power. The ac reactance 11.6 mH is equivalent to 10% at rated reactive power. The control parameters are given in Table III.

TABLE III
CONTROL PARAMETERS

PI-1 : Proportional gain	K_{Cp}	0.1
Integral gain	K_{Ci}	1.0
PI-2 : Proportional gain	K_{ip}	0.5
Integral gain	K_{ii}	50
PI-3 : Proportional gain	K_{ip}	25
Integral gain	K_{ii}	100
PI-4 : Proportional gain	K_{ip}	0.1
Integral gain	K_{ii}	1.0
LPF-1 : Time constant	T_1	0.001
LPF-2 : Time constant	T_2	0.2
LPF-3 : Time constant	T_3	0.01
Proportional gain	K_{ip}	30
Limit for Zero Seq. Voltage	V_{Cmax}^*	7000
Limit for neg. seq. Current	V_{NEG}^*	1320

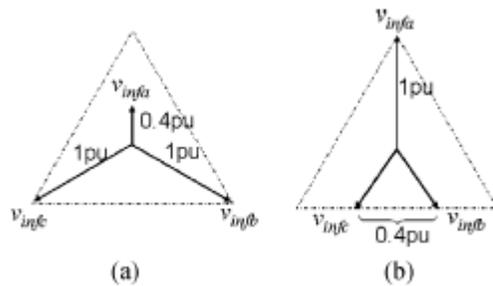


Fig.9.Source voltage under faults. (a)LG. (b)2LS.

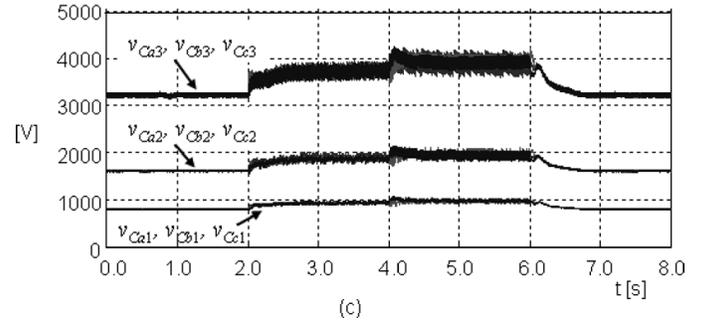
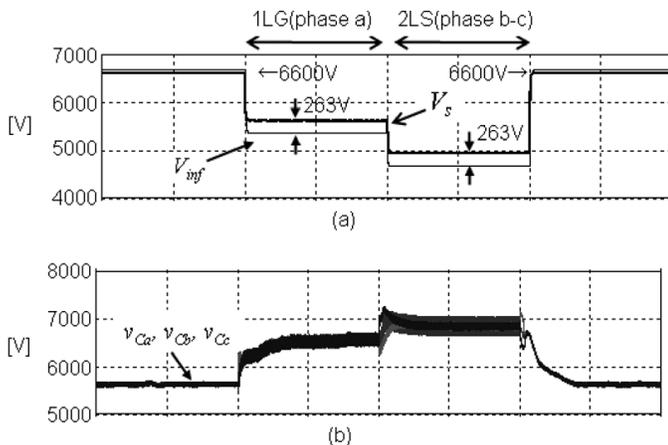


Fig.10. Simulation result of the capacitor voltage
(a) Power system voltage (b) sum of capacitor voltage(c) Each capacitor voltage.

To represent asymmetrical circuit condition, it is assumed that one line grounding (1LG) and two-lines short (2LS) occur in series. The source voltage under these faults is shown in Fig. 9. The simulation result of power system voltage and capacitor voltages are shown in Fig. 10. The STATCOM compensates power system voltage. As a result, grid connection voltage VS is 263 V higher than source voltage during 1LG and 2LS.

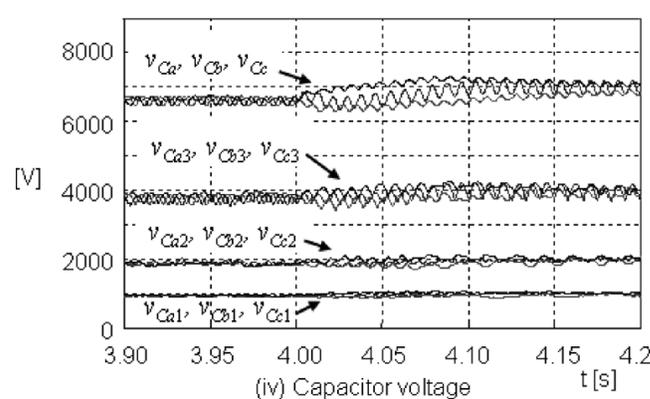
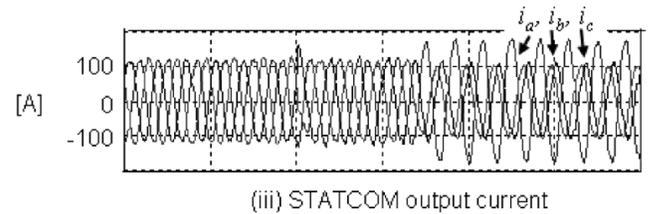
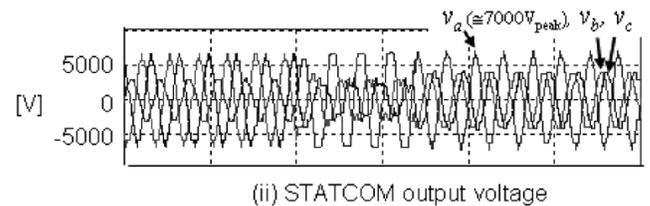
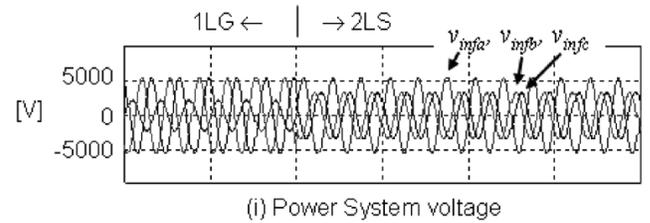


Fig.11.Simulation result (proposal: zero seq. voltage + negative seq. current control for Normal-1LG Fault)

Before 1LG ($t < 2s$), the capacitor voltages of phase clusters are balanced and the voltage ratio of H-bridge cells is controlled to 1:2:4. At the starting point of 1LG ($t = 2s$) and 2LS ($t = 4s$), the capacitor voltages of phase clusters are once unbalanced. But they are rebalanced soon.

Fig. 11 shows the power system voltage, STATCOM output voltage, STATCOM output current and capacitor voltages. Under normal condition or 1LG ($t < 4s$), the zero-sequence voltage method is used and balanced current are output, as shown in Fig. 11(a). The peak value of the currents is about 120A. On the other hand, the negative-sequence current method is used and the STATCOM output unbalanced current under 2LS ($4s \leq t < 6s$), as shown in Fig. 12. By this, the capacitor voltages are balanced. During this time, the peak value of STATCOM output voltage is about 7000 V.

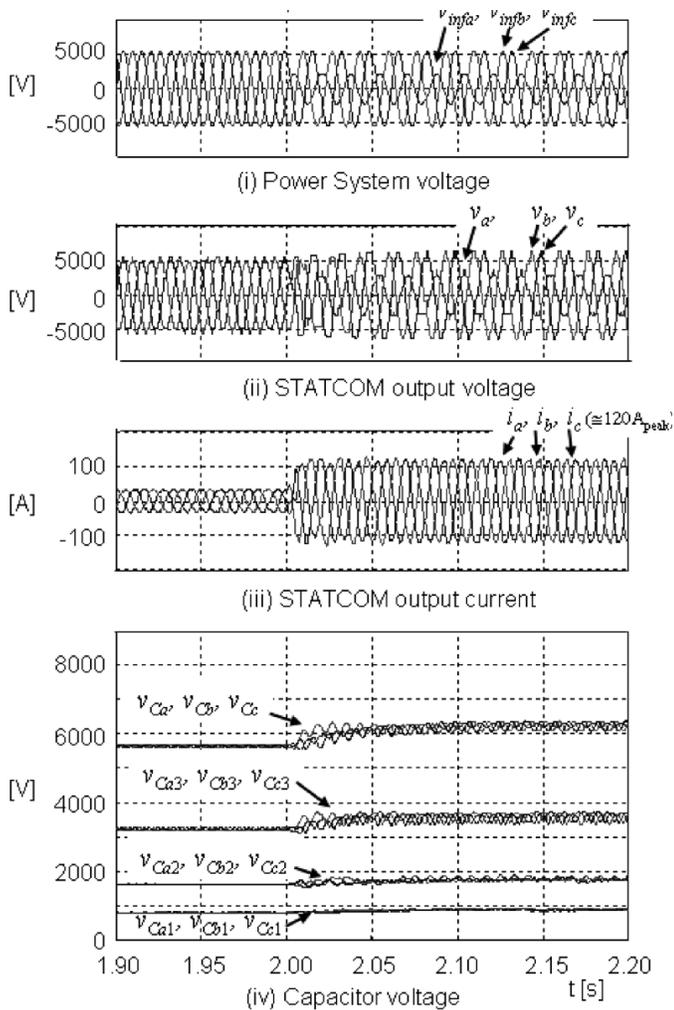


Fig.12.Simulation result (proposal: zero seq. voltage + nega

tive seq. current control for 1LG-2LS Fault)

If the zero-sequence voltage method was used under 2LS, the STATCOM outputs balanced current, as shown in Fig. 13. But the peak value of the STATCOM output voltage is about 8000V. Thus, the STATCOM had to output high voltage and a wide margin of dc capacitor voltage was needed.

As described before, the combination of two capacitor voltage method realizes reasonable circuit design and flexible function of the STATCOM.

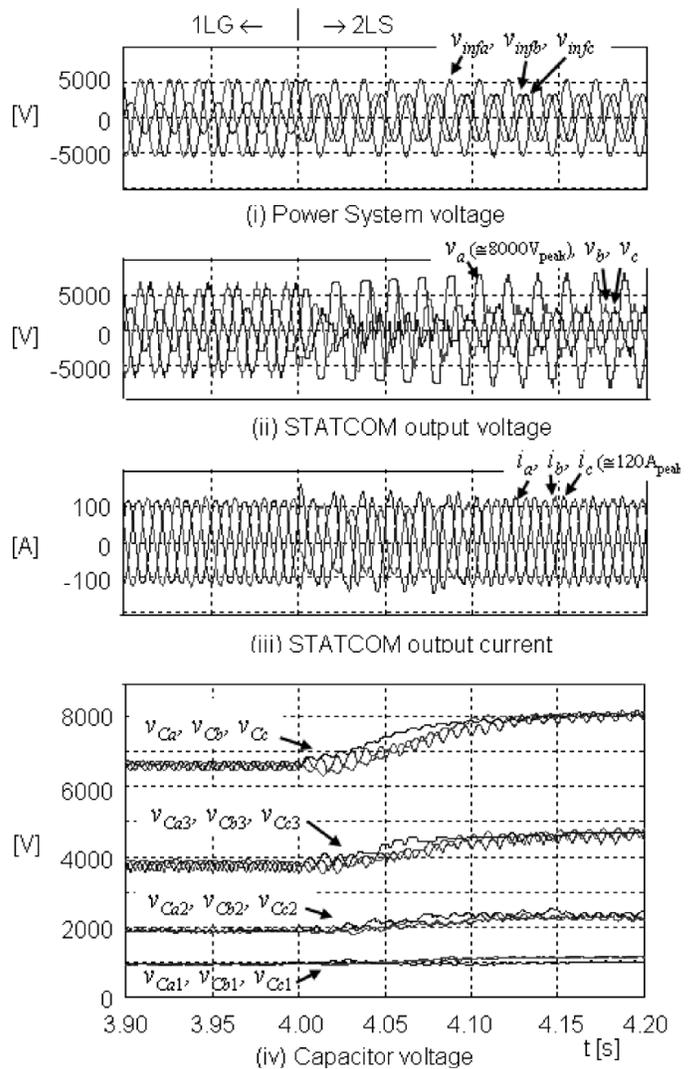


Fig.13.Simulation result (only zero-sequence voltage control)

4. CONCLUSION

This paper presented a configuration and control scheme of cascaded H-bridge STATCOM in three-phase pow

er system. We proposed a control method using zero-sequence voltage and negative-sequence current. The two methods are used exclusively depending on the extent of voltage unbalance. By this method, STATCOM can operate flexibly under normal power system condition and does not need wide margin of dc capacitor voltage under large asymmetrical condition. The validity is examined by digital simulation under one line and two-lines fault circuit condition. The simulation results showed the effectiveness of proposed STATCOM. In addition, proposed control scheme can be used for other type of applications, such as PV (photovoltaic) inverter systems. It expands applicable scope of cascaded H-bridge multilevel converter.

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